

.Amendments to the Drawings:

In the DRAWINGS Section, please renumber Fig. 9 to Fig. 9a and add Fig. 9b presented in the attached Replacement Sheets

Fig. 9b marks the areas of the Threshold Circuit, the Set of Switching Stages and the Set of Capacitors with dotted frames. Similar Fig. 15b marks the separate circuit section of the Set of Capacitors, which is possibly placed on a separate semiconductor substrate, with a dotted frame.

Attachment: Replacement Sheet for Fig. 9a; and Fig. 15a

New Sheet for Fig. 9b and Fig. 15b.

REMARKS/ARGUMENTS

In response to the subject Office Action, an Amendment to the Specifications and to the Claims section is herein submitted.

Examiner Michael Rutland-Wallis is thanked for thoroughly reviewing the above referenced patent application, and for the indication of allowability once various formal matters and informalities are corrected.

Remark on the “*Information Disclosure Statement*”

Attached is form 1449 which was submitted with the Information Disclosure Statement that was mailed to the Patent Office on 01/26/2004. The Examiner is asked to now consider all information contained therein.

Remark on the “Specification”

The correct references and filing dates, not available at the time of initial release of the application, are now entered, identifying applicants copending applications.

Remark on the “Drawings”

Regarding the objection of claims 4, 5 and 22, two new drawings Fig. 9b and Fig. 15b are added. Fig. 9b marks the circuit sections of the Threshold Circuit, the Set of Switching Stages and the Set of Capacitors with a dotted frame to identify these circuit sections. Additional description for Fig. 9b is provided as follows:

Fig. 9b identifies the major circuit sections within the circuit of **Fig. 9a**: the Threshold Circuit is marked **ThrC**, the Set of Switching Stages is marked **SoSWST** and the Set of Capacitors is marked **SoCAPS**.

The Specification and drawings are further enhanced to better identify the circuit section which is possibly positioned on a separate semiconductor substrate. Added **Fig. 15b** identifies the circuit section of the Set of Capacitors which might be produced on a separate carrier. The connecting points (Conn) to the separate carrier were already shown in the original Fig. 15, however their purpose was less obvious. The following additional description is provided for **Fig. 15b**:

Fig. 15a suggests, said set of capacitors could be integrated together with the capacitor switching stages on the same semiconductor substrate. However, such capacitors **Cap 1** to **Cap n** could, for example, be discrete metal or polymer capacitors, on a common planar carrier or they could be integrated on their own semiconductor substrate, which is separate from the semiconductor substrate of said capacitor switching stages. Manufacturing the capacitors in a different process than by integrating the capacitances together with the switch control circuit on the same semiconductor substrate, could lead to significant better quality of the capacitors. The circuit sections of said Set of Capacitors, that could be produced on a separate carrier, is marked **SoCAPS** on **Fig. 15b**; said separate carrier then connects to the remainder of the whole circuit through the connectors **Conn**.

Remarks and Arguments on “Claim Rejections due to 35 USC §112”

Reconsideration of the objection of claims 1-30, as being indefinite and for failing to particularly point out and distinctly claiming the subject matter which applicant regards as the invention. is requested, based on the following:

To add clarity and remove inconsistencies, informalities and lack of antecedent basis, as kindly identified by the examiner, many corrections to the claims are made, specifications and the claims are rephrased in many areas, and the sequence of some

paragraphs or phrases is changed. Thorough care was taken not to introduce any new matter.

In the specification, additional explanation on applicant's invention is provided, as follows:

The variable capacitor arrangement implements a set of small capacitors, a set of capacitor switching stages and a circuit to provide a tuning voltage. To achieve the goal of high Q-factor, the disclosed invention adds circuits and methods to linearize the capacitance change and to minimize the effect of parasitic resistance in the capacitor switching elements, which would degrade the Q-factor.

Within said set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET-transistors as switching device, one per capacitor. The switching operation of such FET-type transistor can be divided into three phases: the fully-switched-off phase (said FET transistor's drain-source-resistance R_{DS} is very high), a steady ramp-up/ramp-down phase or steady transition phase (that is: said FET transistor's resistance R_{DS} is changing between very high resistance and very low resistance in a linear and steady mode) and the fully-switched-on phase (said FET transistor's drain-source-resistance R_{DS} is very low). By thoroughly controlling such switching device within said linear and steady ramp-up/ramp-down phase, the capacitor in series with said switching device is partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

The terms "steady ramp-up/ramp-down phase" or "steady transition phase" (and "steady ramp-up/ramp-down area" or "steady transition area") are used as synonyms throughout this document. The term "area" in this context is used to express the "operating range" – the term "phase" is used to express the "operation in process" within said operating area.

Further, in claims 1, 14, 19 and 29 and wherever it was recited, the "means" limitations are deleted in all cases. In most cases the term "means to ..." is replaced by the term "a circuit to ..."

Regarding claims 1, 14, 19 and 29 the recited phrase "switch said capacitors in parallel" is changed to "connect said capacitors in parallel", to better express, that "said capacitors" are "connected in parallel".

Further regarding claims 1, 14, 19 and 29 recite the limitation "continually switch on" is rephrased. The term "ramp-up/ramp-down" should better explain the linear (and sliding) operation between the 0 % and the 100 % "switched-on" condition. And the additional explanation, recited above, should help to clearly understand the invention.

In addition various inconsistencies and lack of antecedent basis identified by the examiner are now removed, however they are not all commented here in detail.

In the specification, the first paragraph on page 16 is amended to the following:

In accordance with the objectives of this invention, a set of individual capacitors is implemented. Such capacitors Cap 1 to Cap n could, for example, be discrete metal or polymer capacitors, on a common planar carrier or they could be integrated on a semiconductor substrate, either on a separate substrate or on the same substrate as the capacitor switching stages. The advantage of a capacitor not being of the junction (diode) type capacitor is the invariance due to voltage or temperature change at the capacitor.

The words "for example" (see the previous paragraph) are moved from the section "SUMMARY OF THE INVENTION", where they were used in the same context, to the section "DESCRIPTION OF THE PREFERRED EMBODIMENTS". Care was taken not to introduce new matter to this item.

The phrase "either on a separate substrate or on the same substrate as the capacitor switching stages", in the above parasgraph, adds the previously insufficient description of required for claims 4 and 5. This clarification does not add any new matter.

Regarding claim 12, the use of a voltage follower is initially shown in Fig. 6a and is explained in the following:

~~Aln a~~ second solution according to the objectives of this invention, improves the circuit by introducing a voltage follower circuit **Vf** into the circuit of the first solution, as shown in **Fig. 6a**. For a single stage **RDSon** is forced to a linear mode of operation following **Vramp** through the whole working range between the power supply lines. The resulting **RDSon** versus the control voltage **Vramp** is shown in **Fig. 6b**.

Remarks and Arguments on "Claim Rejections due to 35 USC §102"

Applicant respectfully disagrees that Liu shows "a circuit to control the capacitance of a variable capacitor in a linear mode through a steady tuning voltage to achieve (....) comprising a set of small capacitors and a set of switches that is turned on/off depending on the control signals, translinear amplifiers, (....)."

Reconsideration of the rejection of claims 1-2, 8, 12 and 13 as being anticipated by Liu (US Pat. 6,577,180) is requested, based on the following.

Regarding claim 1, the application of Liu actually teaches the concept of a switched capacitor chain, where capacitors are digitally switched in parallel one after the other. Liu uses (digital) comparators to digitally control the switching devices. Liu clearly states, the capacitors are not switched in a linear mode but are switched digitally step by step. See

description of Fig. 5 of Liu. Thus, Liu's concept is very similar to the circuit and method Applicant has mentioned as Prior Art and shown in **Fig. 2a** and **2b**.

Liu explains: "The comparison circuit 50 is an analog-to-digital converter for converting the signals from the voltage dividing circuit 40 into digital signals to control the correction circuit 60." Further, Liu teaches, that the comparison circuit contains (digital) comparators,

Liu explicitly shows a digital ON/OFF-status diagram in FIG. 5 the status of "each correction circuit unit" (the switch) "to be changing to ON or OFF." Concerning the digital switch, please see also Claims 11 and 13 of Liu (US Pat. 6,577,180).

Based on the cited content of Liu's Patent, Liu does not show a partially switched on device with an analog ramp-up/ramp-down operation in his patent; the switch is always either fully switched on or fully switched off in a pure digital manner.

In contrast, the instant application uses operational amplifiers to control the ramp-up/ramp-down operation of the switching devices, in order to switch on a specific capacitor to any value between 0 % and 100 %.

In comparison, Applicant claims (in claim 1.):

A variable capacitor circuit to control the capacitance of a variable capacitor in a linear mode through a tuning voltage and to achieve a high Q-factor at the same time; comprising:

~~means for a set of individual small capacitors;~~

a set of capacitor switching stages, each stage comprising:

~~means for a set of switching devices to continually switch on said capacitors in parallel allowing a steady ramp-up/ramp-down phase between the points of being fully switched on and fully switched off, and where said switching device is connected in series with, one for each of said small capacitors;~~

~~means a switch control circuit to linearly control the switching function operation for each of said set of continuous switching devices in a steady ramp-up/ramp-down manner; means to by generateing a set of controlling signals, directly depending on the a tuning voltage input, one for each of the said capacitor switching stages;~~

~~means a threshold circuit to generate a set of threshold values, one for each of the said capacitor switching stages; and~~

~~means a circuit to provide a tuning voltage, dedicated for the voltage controlled capacitance change.~~

Primarily applicant claims the use of a switch with a steady ramp-up/ramp-down phase, to partially switch (between 0 % and 100 %) a capacitor in parallel to other capacitors of a set of capacitors.

Regarding claim 11, the implementation of a "set of small capacitors", such capacitors may be implemented as integrated capacitors on the same semiconductor chip together with the " set of circuits to control the switching operation" or on a separate semiconductor substrate. It may even be implemented on a separate carrier as a multi-capacitor arrangement or it may even be implemented as individual components. The presented patent application is not limited to a specific implementation of a set of capacitors

Remarks and Arguments on "Claim Rejections due to 35 USC §103"

Reconsideration of the rejection of claims 3-7, 9-10 and 14-30 as being unpatentable over Liu (US Pat. 6,577,1.80).is requested, based on the following.

Figure 3 of Liu shows a circuit fundamentally different from the instant application, as Liu does not implement a linear ramp-up-ramp-down operation of the switching device to achieve a sliding (0% to 100%) parallel connection of the small capacitors. Liu implements (digital operating) comparators in contrast to the (linear operating) operational amplifiers of the instant application.

In the present application, the various techniques to manufacture and connect the Set of Capacitors to the Set of Capacitor Switching Stages are not the key of the invention, however they are claimed as an important characteristic of the invention, in order to not limit the embodiment of said capacitors being integrated onto the same semiconductor substrate as said capacitor switching stages.

Reconsideration of the above rejection (or objection) is therefore respectfully requested.

All claims are now believed to be in condition for allowance, and allowance is so requested.

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'SBA', with a stylized flourish at the end.

Stephen B. Ackerman, Reg. No. 37,761